

NMRA Conformance Testing of Decoders

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Introduction

As many of you know, NMRA has established a testing and conformance program of DCC decoders to assure our membership that a certified decoder will work with their individual DCC equipment. The purpose of this article is to help you understand what goes into this testing and the limitations associated with this testing.

The purpose of Standards and Recommended Practices that have been developed by NMRA, interested manufacturers and expert users is to establish “standards for the better interchange and operation of model railroad equipment”.

Nowhere is this more important than in the relatively new area of Digital Command Control. Whereas many mechanical Standards and RPs can be checked and verified by users of the equipment, the same can not be said for the electronics of DCC. For mechanical measurements, such as wheels and track, the NMRA Gauge was developed and is available to sale at most hobby shops. For DCC measurements, the same is not true.

Recently, PRICOM has developed and sells a testing device called the “DCC Pocket Tester”. This device can perform simple tests on the track to insure the DCC signal is correct.
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To insure reliable interchange, special testing equipment, not normally available to the average model railroader, must be used. As a result, the Conformance and Inspection Group (C&I) of the Standards and Conformance Department of the NMRA has developed special testing equipment and procedures to test the minimum characteristics of a decoder to insure it will work on a layout with a DCC Command System that also has a NMRA Conformance Warrant. This “DCC Decoder Test Board” is available for sale from the NMRA. However, it will shortly be replaced by a newer, more sophisticated test board that will provide more extensive testing.

This article is a brief description of the tests that are performed by the C&I Group. Testing of a decoder is done in two major areas – Baseline Testing and Recommended Practices Testing. The Baseline tests test that the decoder conforms to the NMRA DCC standards S9.1 and S9.2. A conforming decoder must read correct signals on the track and properly respond to them. A conforming decoder must also be able to deal with signals and commands that are not perfect. Imperfections in wiring, dirty track, marginally performing Command Stations, and other equipment on the rails can all contribute to weak or distorted signals. The decoder itself can also contribute to signal problems.

Baseline Test Suite

The Baseline test suite is performed to insure the decoder will respond to a legitimate signal on the track and reject an improper signal on the track. The equipment used to perform the tests will be described followed by a brief description of each test together with the reason the test is important for proper decoder conformance.

Baseline Packet Structure

But first, a brief explanation of the DCC signal on the track is in order. Figure 1: Baseline DCC Signal on Track is composed of four parts – Preamble, Address Data Byte, Instruction Data Byte, and Error Detection Data Byte. As with any electronic device, decoders only understand two conditions – Ones and Zero. These two conditions are expressed by the width of the square wave. For One bits, the width of the signal can vary from 52 micro-seconds, uS, to 64 uS. For the Zero bits, the minimum width is 90 uS up to 1,200 uS. By the way, “stretching” the Zero bit to a value greater than 95 uS allows non-DCC equipped locomotive to run on a DCC layout.

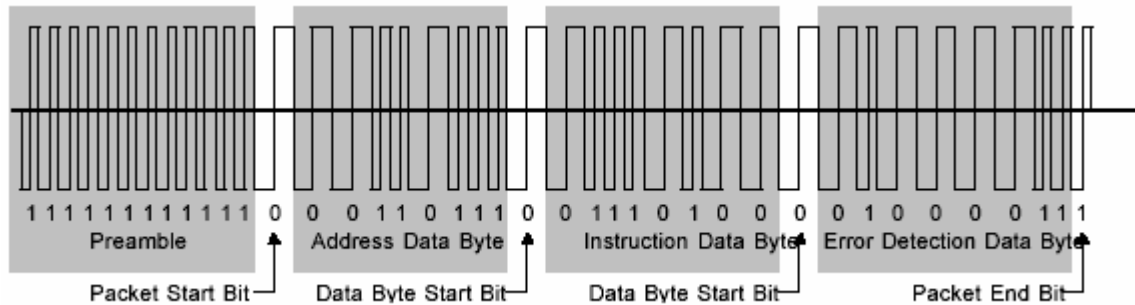


Figure 1: Baseline DCC Signal on Track

This “perfect” DCC signal is not always possible – given our electronic skills, or lack of skills, to build the perfect layout. Therefore, some tolerances have been built into the standards that the decoder must be able to accept and react properly.

With this in mind, the following tests were formulated to understand the ability of the decoder to detect a legitimate DCC signal and react to it properly. The indented text is taken directly from the testing manual.

General Baseline Packet Test Sequence Types

This section discusses the two general types of packet test sequences.

Packet Acceptance Test Sequence

This test sequence is used for packet acceptance tests. This test sequence tests if the decoder will properly accept and act on a single command packet as long as the bit timing as specified in S9.1 is correct. This form of test also verifies that the decoder accepts a single packet even if it is preceded or followed by various types of valid and invalid bit sequences.

Figure 2: Packet Acceptance Test Sequence shows a sketch of the baseline packet acceptance test sequence.

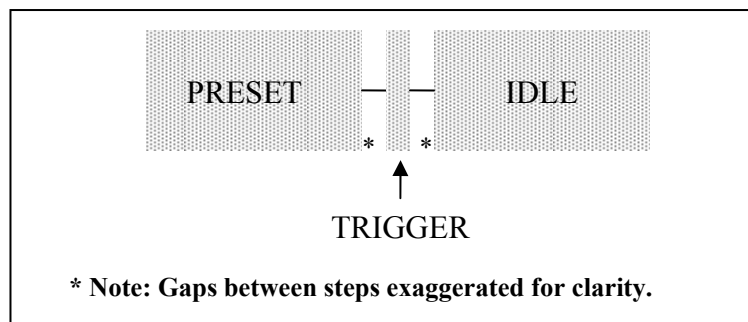


Figure 2: Packet Acceptance Test Sequence

Each baseline packet acceptance test sequence consists of these steps:

1. PRESET – This step sends one second of commands to preset the decoder output to a state the tester can recognize. The command is different depending on whether we are testing a mobile, accessory, or lamp only decoder. The output state of the decoder is tested at the end of this step.
2. TRIGGER – This step sends a single command to change the output state of the decoder. The decoder is expected to act on a single occurrence of a valid command addressed to the decoder.
3. IDLE – This step consists of 1 second of idle commands to give the decoder output time to respond to the trigger command. The output state of the decoder is tested at the end of this step.

Packet Rejection Test Sequence

This test sequence tests if the decoder will properly reject a sequence of command packets as long as they are invalid in some way such as having a wrong address or an incorrect bit.

Figure 3: Packet Rejection Test Sequence shows a sketch of the general baseline packet acceptance test sequence.

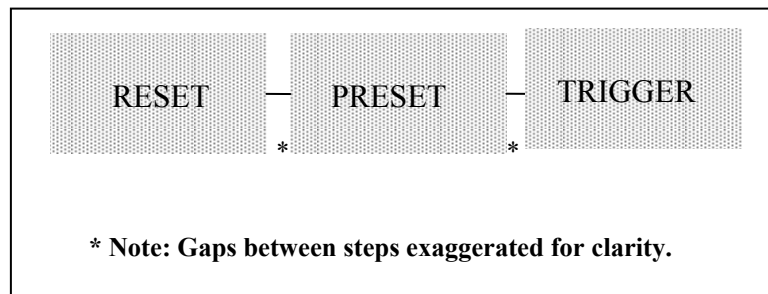


Figure 3: Packet Rejection Test Sequence

Each baseline packet rejection test sequence consists of these steps:

1. **RESET** – This step sends one second of decoder reset packets. This is used to reset the decoder to a known state. The output state of the decoder is tested at the end of this step.
2. **PRESET** – This step sends one second of commands to preset the decoder output to a state the tester can recognize. The command is different depending on whether we are testing a mobile, accessory, or lamp only decoder. The output state of the decoder is tested at the end of this step.
3. **TRIGGER** – This step sends one second of commands that attempt to improperly change the state of the decoder. The decoder is expected to reject multiple occurrences of invalid commands or commands addressed to another decoder. The output state of the decoder is tested at the end of this step.

Baseline Test Equipment

Figure 4: Baseline Test Equipment Overview is a photographic overview of the test system. Figure 5: Baseline Test Equipment Close-Up is a close-up of the test hardware.

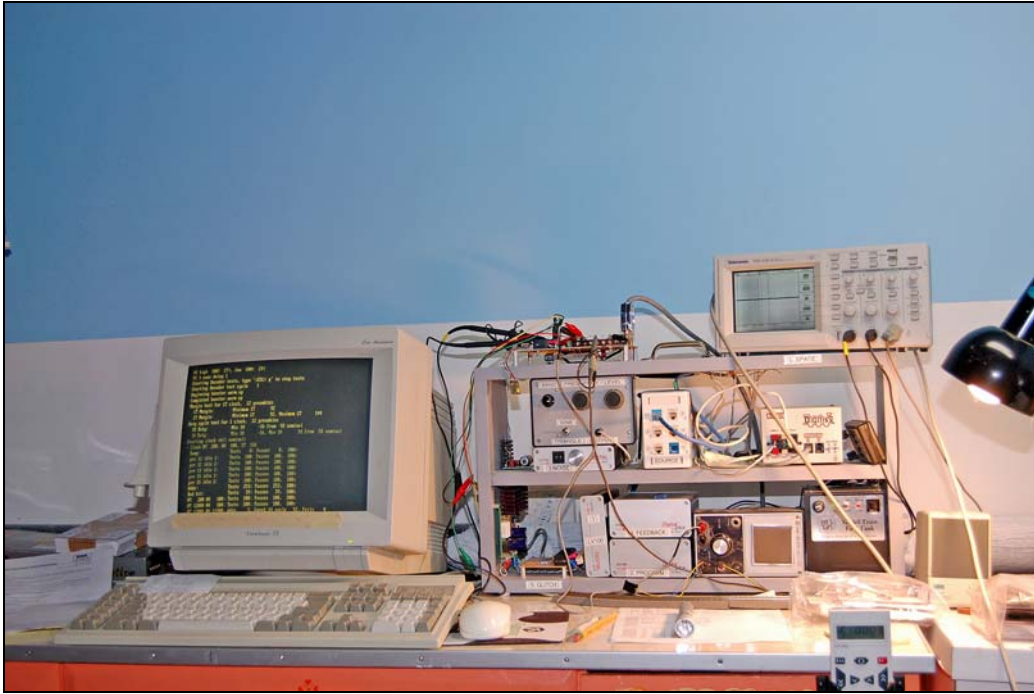


Figure 4: Baseline Test Equipment Overview

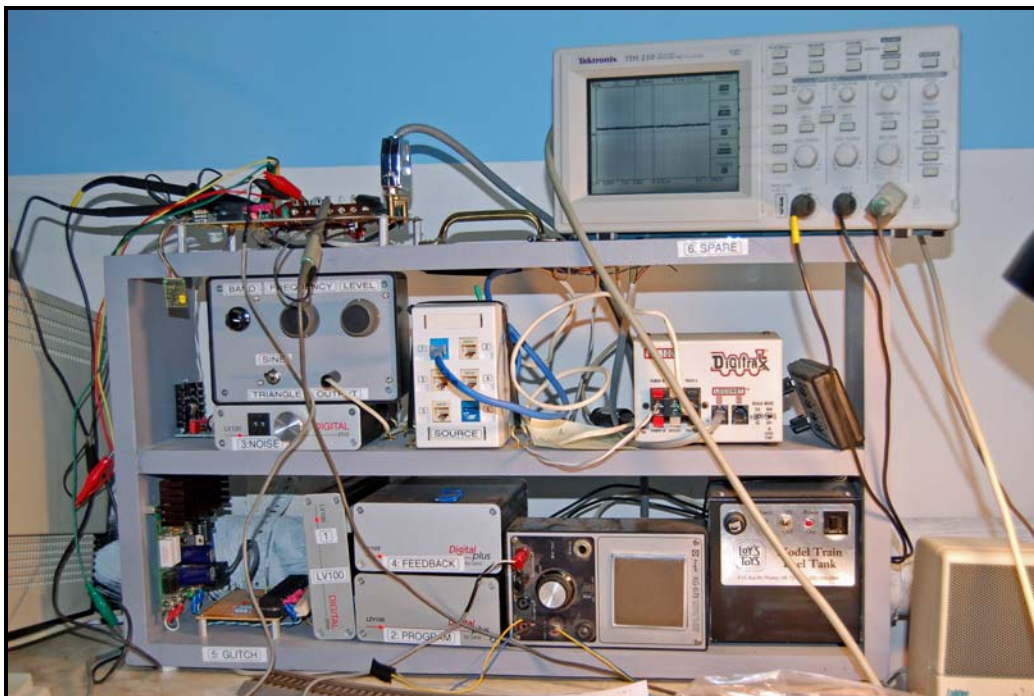


Figure 5: Baseline Test Equipment Close-Up

The system can connect to a variety of different types of decoders for test. The system also quickly connects a variety of normal, noise injecting, and glitch injecting boosters to the decoder. Figure 6: Baseline Test Equipment Diagram shows the equipment used to conduct baseline tests.

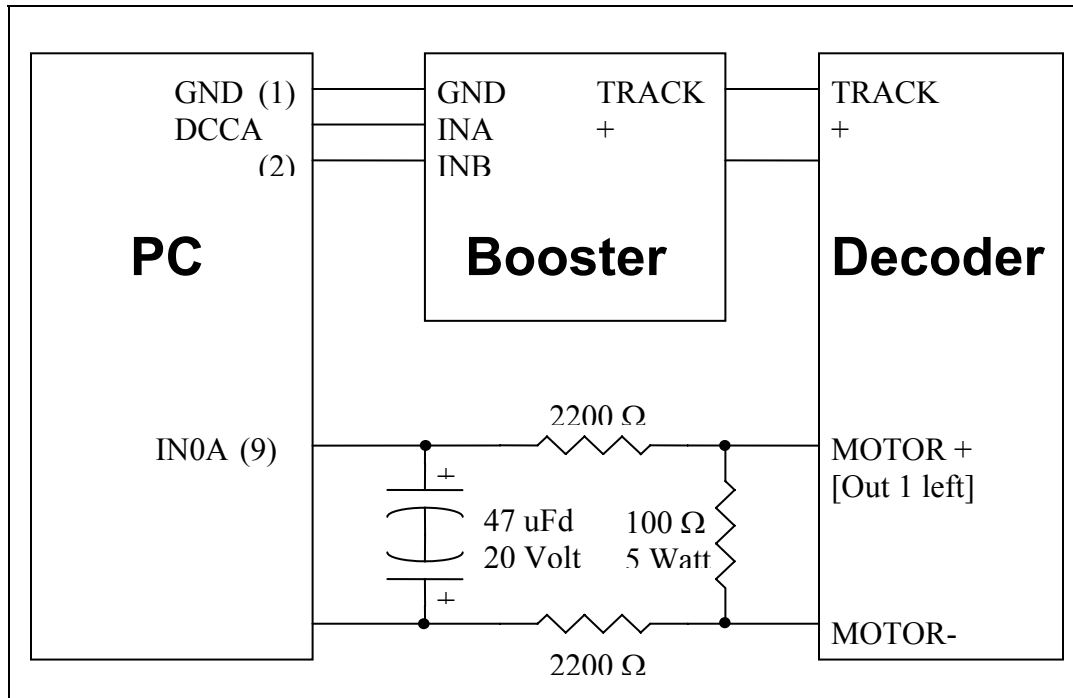


Figure 6: Baseline Test Equipment Diagram

There are 4 components used for baseline tests:

1. The test controller PC. This consists of a PC compatible computer and a specially designed sender board capable of sending a variety of good and bad DCC packets. The sender board can also receive decoder responses using the INxx inputs.
2. A selection of DCC test boosters. 3 types of boosters are used for decoder testing:
 1. A NMRA conformant test booster. This booster is used first to verify the decoder works with conformant DCC signal levels, rise times, etc.
 2. A test booster capable of varying the DCC signal level, rise and fall times, and 200 KHz. noise of the DCC test signal. The booster verifies that a decoder works at the worst case signal level, rise and fall times, and 100 KHz nose.
 3. A test booster capable of injecting a crossover glitch into the DCC test signal. This booster verifies that the decoder can tolerate a glitch that occurs as the signal crosses the 0 Volt point.
3. A decoder under test. The Baseline test equipment can test 3 types of decoders:
 1. A mobile decoder with a motor control output. This decoder is tested by sending DCC commands that change the motor output and then verifying that the decoder correctly handled the command.

2. A mobile decoder with a function output. This decoder is tested by sending DCC commands that change a function output and then verifying that the decoder correctly handled the command.
3. An accessory decoder. This decoder is tested by sending DCC commands that change an accessory output and then verifying that the decoder correctly handled the command.
4. An RC network to filter the decoder output. This network removes any high speed transients from the decoder output signal and then passes it to the test input of the test control PC.

Baseline Tests

1. DCC One Margin Test

This test determines the minimum and maximum 1 bit times that the decoder will accept. It sets the 0 bit time to the nominal value and then changes the 1 bit time up and down to determine the range. It does this by using a version of the packet acceptance test described in section 3.2 to verify that the decoder will pass 100% of the packets for a given value of 1 bit time. It uses a binary search algorithm to select the next 1 bit time to test and then runs the packet acceptance test for 100 cycles or until a failure occurs.

This test changes the width of the 1 bit to the limits of 52 uS and 64 uS and beyond. Although the Command Station is required to send 1 bits within the tighter limits of 55 uS to 61 uS, the signal can degrade as it progresses along the track. Therefore, the 1 bit limits for the decoder were widened to accommodate this degradation. The decoder should be able to recognize 100% of the 1 bits within the stated limits above.

2. DCC One Duty Cycle Test

This test determines the minimum and maximum 1 bit duty cycle that the decoder will accept. It sets the 0 bit time to the nominal value and then changes the 1 duty cycle up and down to determine the range. It does this by using a version of the Packet Acceptance Test described in paragraph 3.2 to verify that the decoder will pass 100% of the packets for a given value of 1 duty cycle. It uses a binary search algorithm to select the next 1 bit time to test and then runs the packet acceptance test for 100 cycles or until a failure occurs.

The total 1 bit duty cycle is actually the time for the signal to rise from 0 volts to maximum plus volts, drop to maximum negative volts and return to 0 volts. This time is not typically double the time for the 1 bit time above zero since the timing of the bit below zero can differ from that above zero. The decoder must recognize this difference and understand when a legitimate 1 bit duty cycle has been sent.

The decoder should be able to recognize 100% of the legitimate 1 bit duty cycle within the stated limits to pass.

3. Repetitive DCC Tests

Once it has been verified that the decoder is able to recognize legitimate 1 bit signals, the decoder is subjected to the full packet as illustrated in Figure 1. The Repetitive DCC Tests listed below. Since the decoder is flooded with a series of commands, it is allowed to miss a few. For the decoder to pass these series of tests, it only has to respond to 95 percent of the packets sent.

All of the tests in this section are repeated for a variety of 1 and 0 bit times, 0 stretch values, etc. The 1 and 0 bit times are set and then each test sequence is run. The exact 1 and 0 low and high times are printed out prior to each series. All 1 and 0 bit times are within the specification so all tests should pass for all 1 and 0 bit times.

3.1 Ramp Test

This test sends all valid baseline commands to the decoder and verifies that it responds. The exact tests vary for locomotive and accessory decoders. For locomotive decoders, you can visually verify that the motor and optional lamp states change as shown on the computer screen. For accessory decoders, you can verify that the decoder change's polarity if the decoder provides a status lamp.

The program reads back the Voltage polarity from the decoder output and verifies that it is correct. For locomotive decoders, this is only done for the higher speed steps to make sure the motor Voltage is clearly positive or negative. For accessory decoders, it cycles through each of the possible output pairs and also cycles the active bit on and off.

3.2 Packet Acceptance Test

The packet acceptance test verifies that at least 95% of good packets are properly received by the decoder. For locomotive decoders, the test begins by presetting the decoder to one half speed reverse. This is done by repeatedly sending the proper reverse speed command. The program then verifies that the motor Voltage is correct. Next, the program sends the appropriate number of idles for that test cycle, one emergency stop command with the appropriate number of preamble bits, and one second of idle commands. The idle commands are sent to give the decoder time to stop the motor. The program then verifies that the motor has stopped. This sequence is repeated 100 times, at least 95 of which must pass.

For accessory decoders, the test begins by presetting the decoder to activate the switch in one direction. This is done by repeatedly sending the proper accessory command. The program then verifies that the output Voltage is correct. Next, the program sends the appropriate number of idles for that test cycle, one command with the appropriate number of preamble bits to reverse the switch state, and one second of idle commands. The idle commands are sent to give the decoder time switch state. The program then verifies that the decoder has switched state. This sequence is repeated 100 times, at least 95 of which must pass.

The overall 100 test sequence is repeated for different numbers of interpacket idles and different numbers of packet preamble bits. These idle and preset counts are displayed in the test log and summary files

3.3 Bad Address Test

This test verifies that the decoder only responds to its address and no others. It uses the same preset and trigger commands used for the locomotive and accessory packet acceptance test described in paragraph 3.2. The program begins each test cycle by presetting the decoder to the initial state. It then switches to an incorrect address and attempts to change the state using one second of commands that are correct except for the address. In no case should the decoder switch state.

This test is repeated for each invalid address. A final test is then done with the valid address to verify that the decoder is responding to a good command.

3.4 Bad Bit Test

This test verifies that the decoder rejects all commands with a single wrong bit. It tests all bits in a packet from the first bit of the preamble to the last bit of the checksum.

Each test cycle begins by presetting the decoder as in the packet acceptance test. A command to change state with one wrong bit set is then repeatedly sent to the decoder for a period of one second. A properly working decoder will not respond to this command and change state.

This test is repeated for the preamble, address, command, and checksum portions of a command packet. A final test is then done with all bits valid to verify that the decoder is responding to a good command.

3.4 Single Stretched 0 Test

This test verifies that the decoder will accept a packet with a single stretched 0 in the packet. It is similar to the 3.2 Packet Acceptance Test except that the first 0 after the preamble is stretched by the appropriate amount for that test cycle.

Each test cycle begins by presetting the decoder as in the 3.2 Packet Acceptance Test. A single command to change the state with a stretched 0 is then sent. This is followed by one second of idles. A properly working decoder should accept this trigger packet and work exactly as it did during the '**pre 10 idle 1**' portion of the 3.2 Packet Acceptance Test.

The total length and high time in microseconds of the single stretched 0 is shown in the log and summary files for each test cycle. For example, '**0T 12000 0H 11890**' would be a stretched 0 with a total duration of 12000 microseconds and a high time of 11890 microseconds.

4. Truncated Packet Test

This test is not run by default and is not used to determine pass or fail criteria. It is included to gather data on how decoders accept packets that are preceded by truncated packets.

This test determines if a decoder will accept a trigger packet that is immediately preceded by a truncated packet. It does this by using a version of the packet acceptance test described in paragraph 3.2 to verify that the decoder will accept a trigger packet that is preceded by a packet that is truncated by one bit each test cycle.

5. Prior Packet Test

This test determines if a decoder will accept a trigger packet that is immediately preceded by a packet with various combinations of 0 and 1 bits. It does this by using a version of the packet acceptance test described in paragraph 3.2 to verify that the decoder will accept a trigger packet that is preceded by a packet that has various bits changed each test cycle. A conforming decoder should accept all trigger packets regardless of the type of packet preceding the trigger packet.

6 Byte Prior Packet Test

This test determines if a decoder will accept a trigger packet that is immediately preceded by a 6 Byte packet without a packet end bit. It does this by using a version of the packet acceptance test described in paragraph 3.2 to verify that the decoder will accept a trigger packet that is preceded by a variety of 6 Byte packets without packet end bits. A conforming decoder should recognize these 6 Byte packets as too long to be valid and accept the trigger packet.

7. One Feedback Bit Test

This test determines if a decoder will accept a trigger packet that is immediately preceded by a packet with 1 inter Byte 0 replaced by a feedback bit. It does this by using a version of the packet acceptance test described in paragraph 3.2 to verify that the decoder will accept a trigger packet that is preceded by a packet that has various bits changed each test cycle. A conforming decoder should accept the trigger packet even if the previous packet has an inter Byte 0 bit converted to a feedback bit.

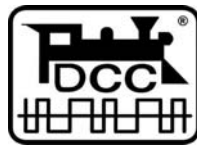
8. Two Feedback Bits Test

This test determines if a decoder will accept a trigger packet that is immediately preceded by two feedback bits. It does this by using a version of the packet acceptance test described in section 0 to verify that the decoder will accept a trigger packet that is preceded by a packet that has various bits changed each test cycle. A conforming decoder should accept the trigger packet even if it immediately preceded by two feedback bits. The two feedback bits are inserted immediately after the packet end bit of the last preset packet and are immediately followed by the preamble of the trigger packet.

Conclusion

As you can see, the testing of decoders is quite complex and is not for the lighthearted. It would be very difficult for the typical modeler to understand why a particular decoder is not responding to instructions from the Command Station. Therefore, NMRA has taken on the role of testing DCC equipment to insure it conforms to the established Standards and Recommended Practices. With this conformance comes our assurance that the decoder will operate properly with other DCC equipment that also has passed conformance.

When you purchase a particular piece of DCC equipment, look for the following two logos on the packet.



These two symbols means the product has been certified by the manufacturer and verified by the Standards & Conformance Department of the NMRA as compatible with and conforms to the NMRA Standards and Recommended Practices.